

FIG. 1

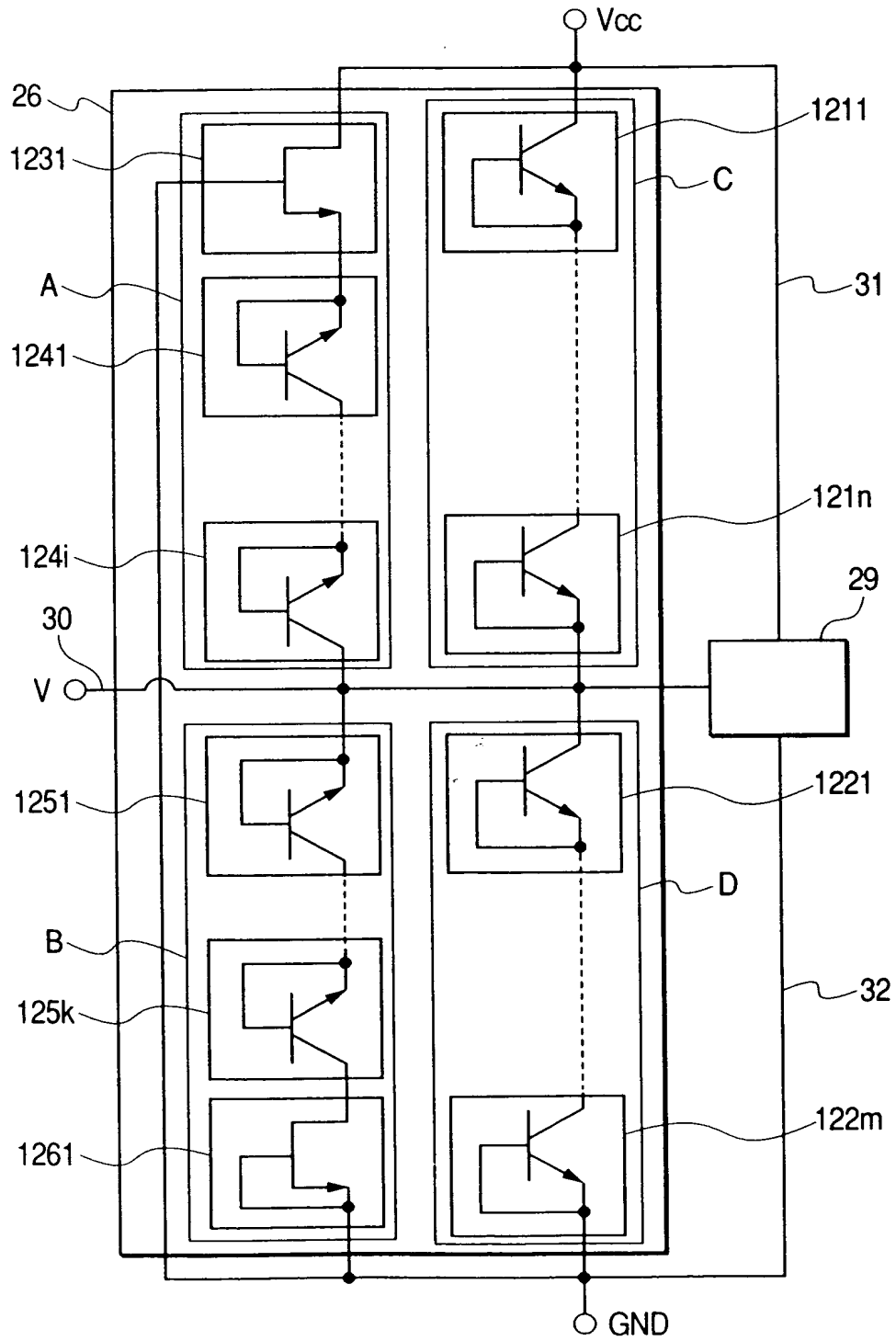


FIG. 2(A)

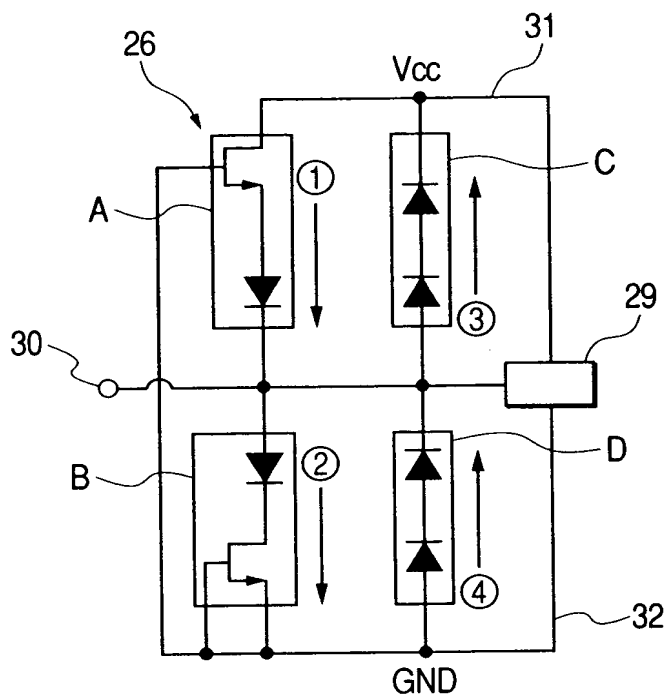


FIG. 2(B)

No.	NOTED PIN & POTENTIAL DIFFERENCE	CURRENT PATH
1	Vcc(+), GND(-)	① → ②
2	Vcc(+), S(-)	①
3	S(+), GND(-)	②
4	Vcc(-), S(+)	③
5	Vcc(-), GND(+)	④ → ③
6	S(-), GND(+)	④

FIG. 3

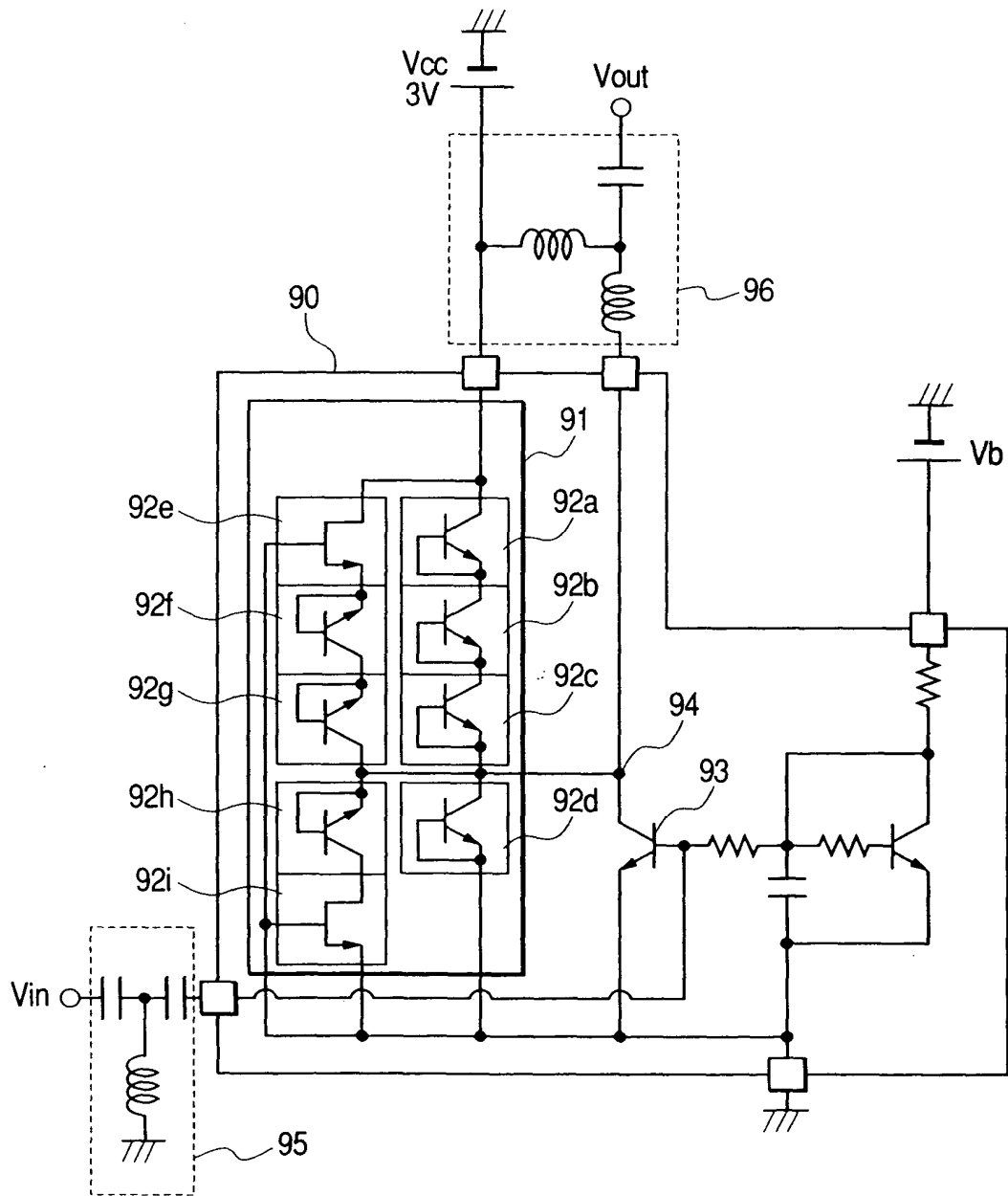


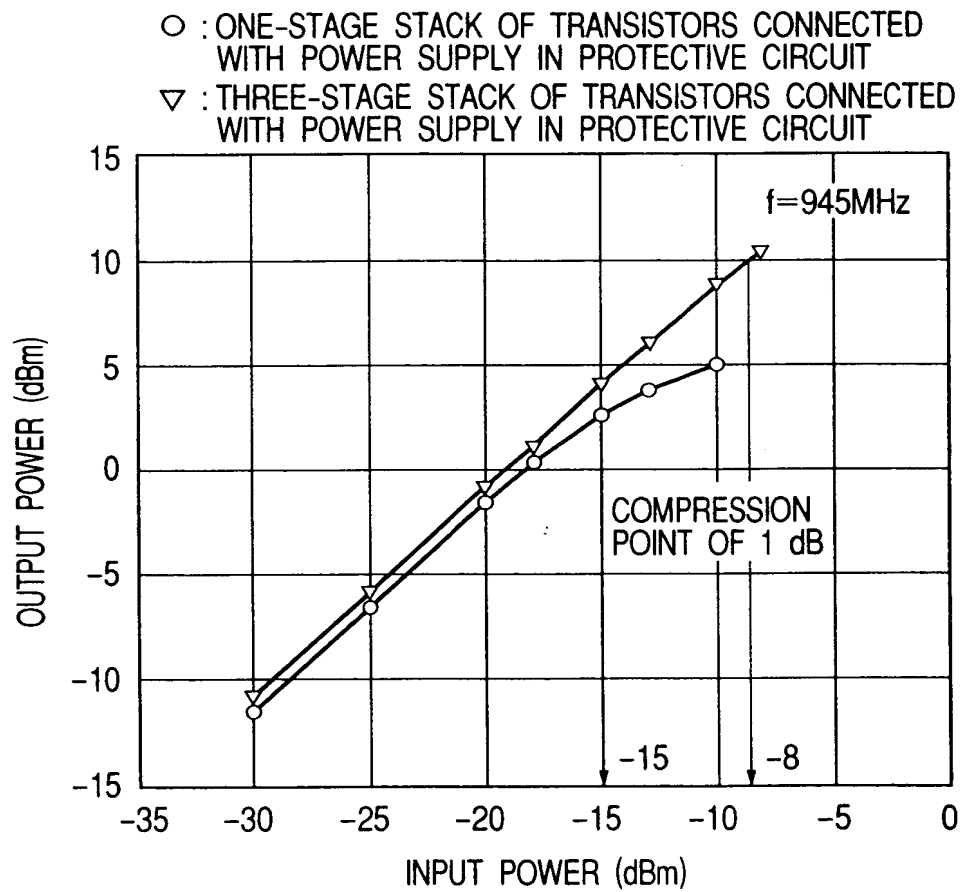
FIG. 4

FIG. 5

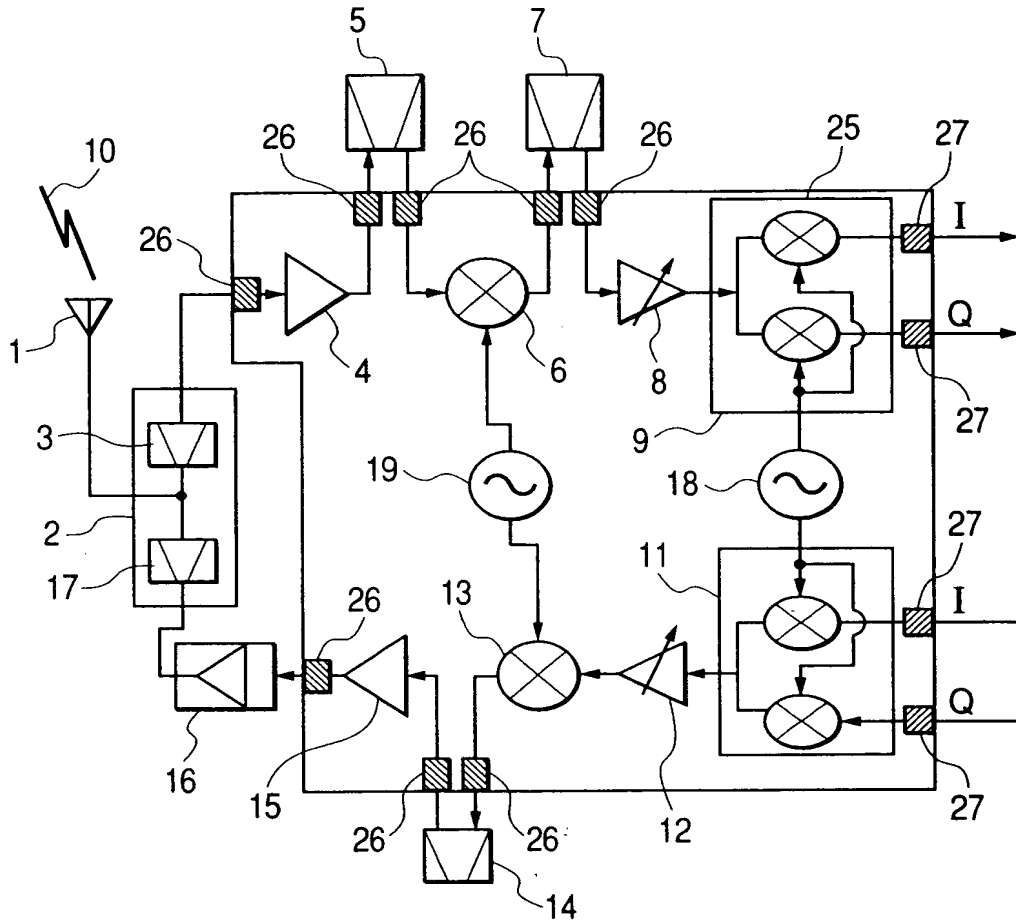


FIG. 6

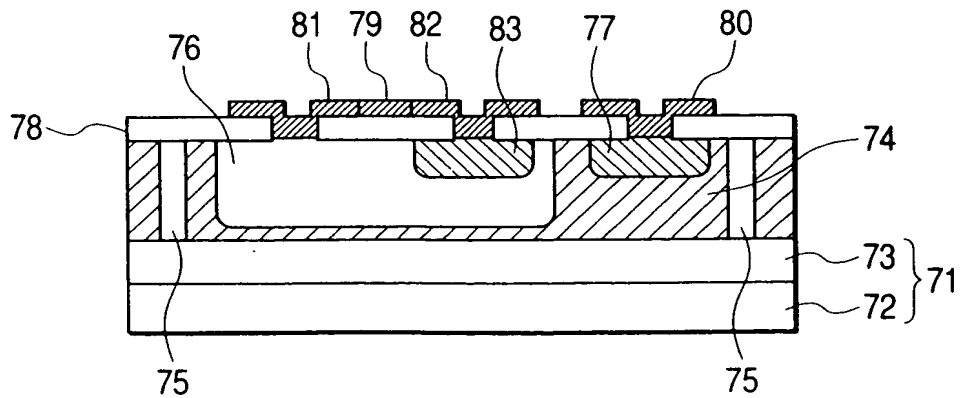


FIG. 7

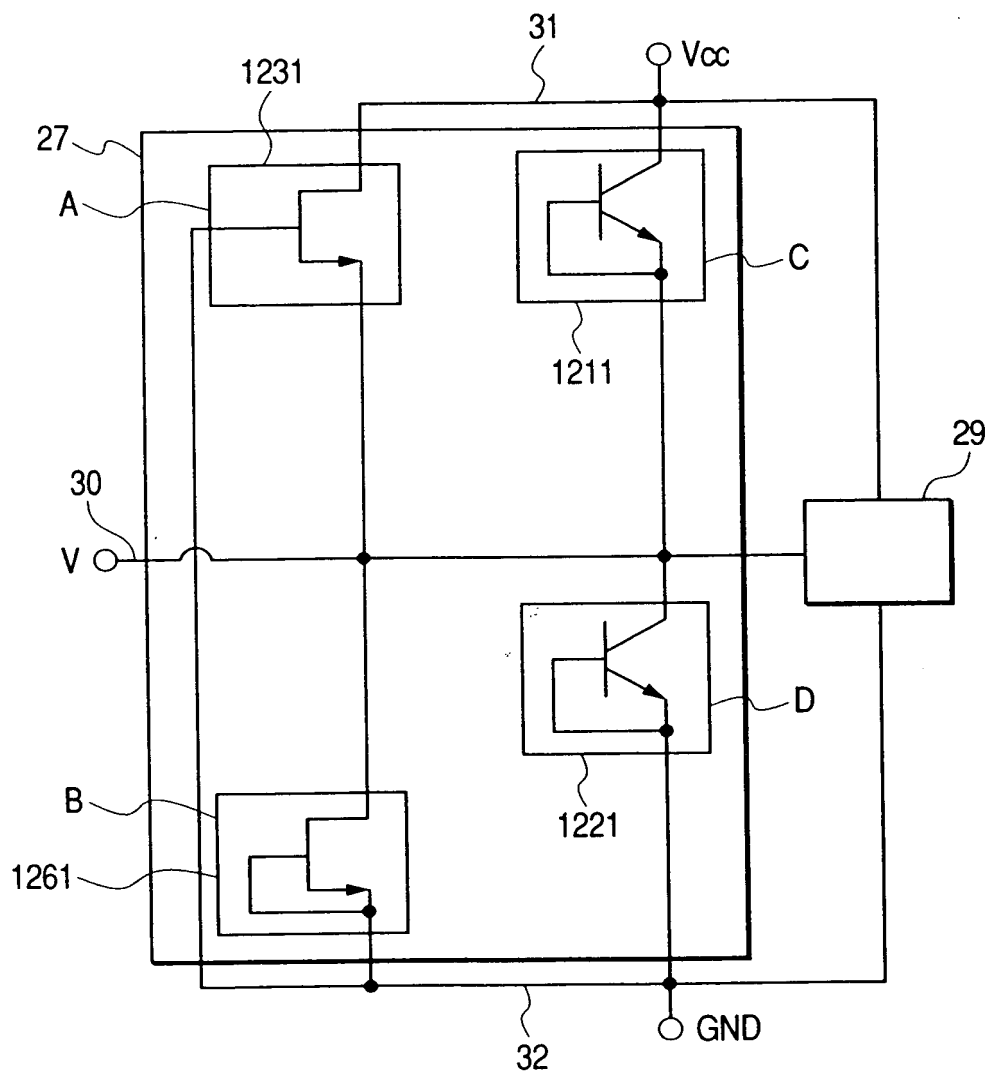


FIG. 9

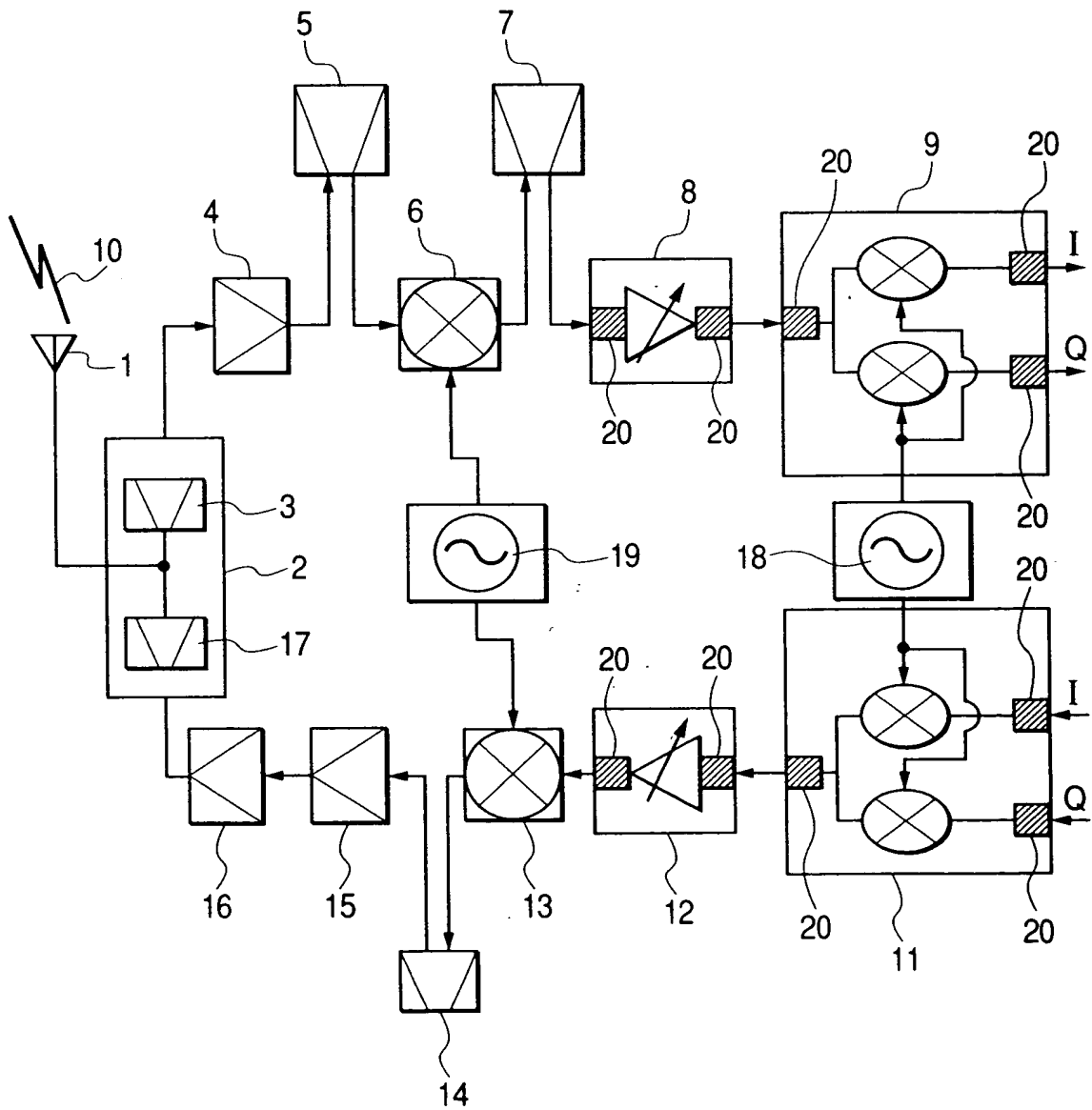


FIG. 10

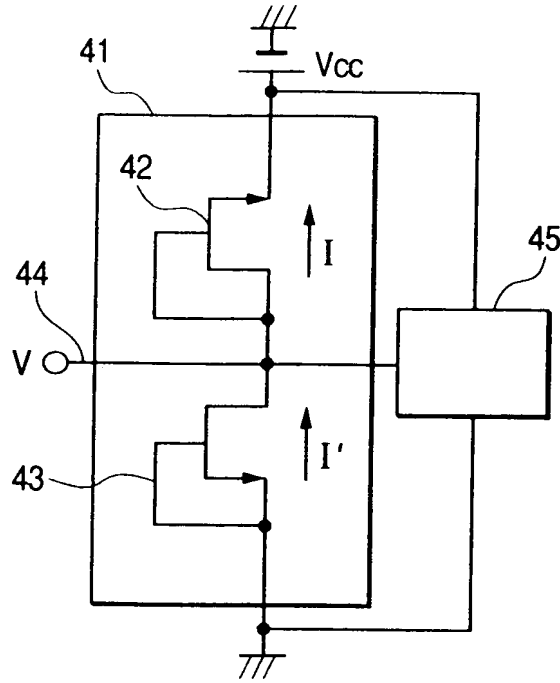


FIG. 11
PRIOR ART

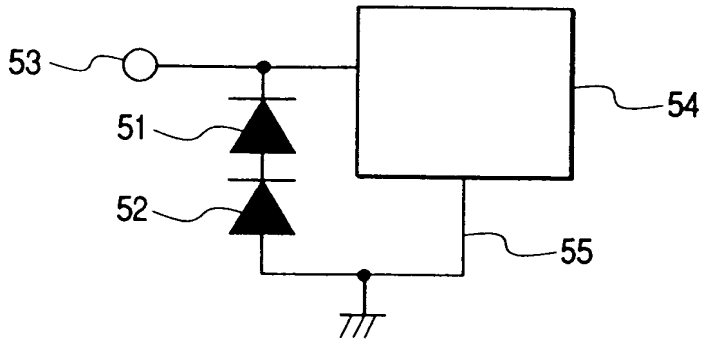


FIG. 12

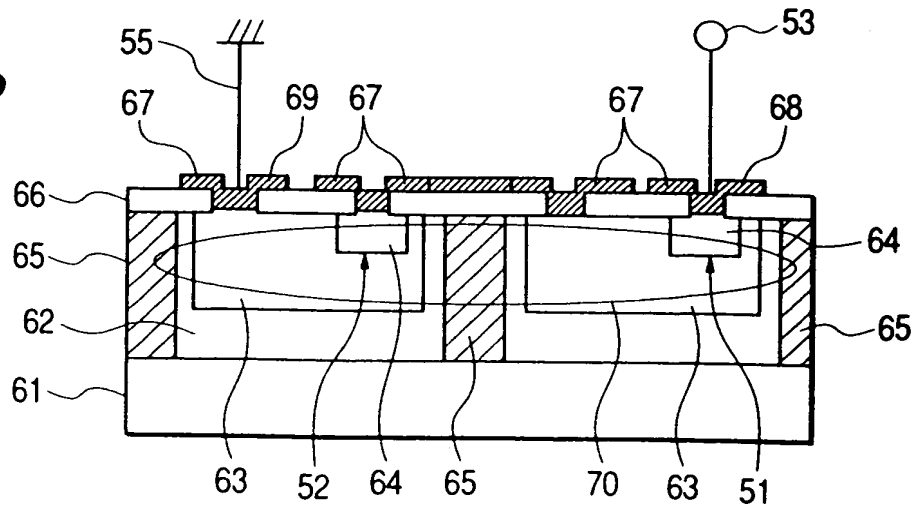


FIG. 13(A)

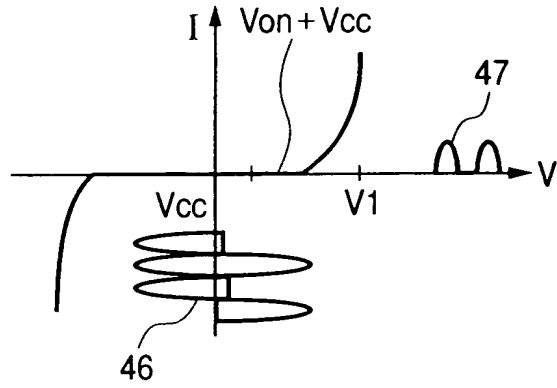


FIG. 13(B)

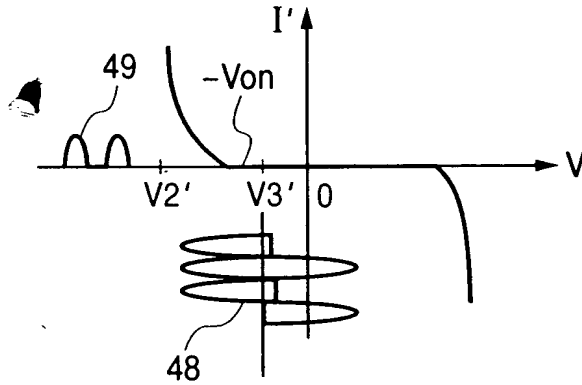


FIG. 14

